10-09-01

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# UTILITY PATENT APPLICATION TRANSMITTAL
**(Only for new nonprovisional applications under 37 CFR 1.53(b))**

| | | |
|---|---|---|
| Docket No. | : | 47426/RJP/B600 |
| Inventor(s) | : | Myles H. Wakayama |
| Title | : | LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS |
| Express Mail Label No. | : | EL 717376625 US |

**ADDRESS TO**: Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

Date: October 5, 2001

1. X **FEE TRANSMITTAL FORM** *(Submit an original, and a duplicate for fee processing).*

2. **IF A CONTINUING APPLICATION**

 X This application is a continuation of patent application No. 09/649,197.

 Prior application information: Examiner S. Grimm; Group Art Unit: 2817

 ___ This application claims priority pursuant to 35 U.S.C. §119(e) and 37 CFR §1.78(a)(4), to provisional Application No. .

3. **APPLICATION COMPRISED OF**

**Specification**

 21 Specification, claims and Abstract (total pages)

**Drawings**

 4 Sheets of formal drawing(s) (FIGS. 1 to 5)

**Declaration and Power of Attorney**

 ___ Newly executed

 ___ Unexecuted declaration

 X Copy from a prior application (37 CFR 1.63(d))(for continuation and divisional)

4. ___ **Microfiche Computer Program** *(Appendix)*

5. ___ **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, all necessary)*

 ___ Computer Readable Copy

 ___ Paper Copy (identical to computer copy)

 ___ Statement verifying identity of above copies

6. **APPLICANT(S) STATUS UNDER 37 CFR § 1.27**

 ___ Applicant(s) and any others associated with it/them under § 1.27(a) are a SMALL ENTITY

## UTILITY PATENT APPLICATION TRANSMITTAL
**(Only for new nonprovisional applications under 37 CFR 1.53(b))**

Docket No.: 47426/RJP/B600

**7. ALSO ENCLOSED ARE**

_X_ Preliminary Amendment

___ Includes "Cross-Reference to Related Applications"

___ A Petition for Extension of Time for the parent application and the required fee are enclosed

___ An Assignment of the invention with the Recordation Cover Sheet and the recordation fee are enclosed

_X_ This application is owned by Broadcom Corporation pursuant to an Assignment recorded at Reel 010252, Frame 0828

___ Information Disclosure Statement (IDS)/PTO-1449

___ Copies of IDS Citations

___ Certified copy of Priority Document(s) *(if foreign priority is claimed)*

___ English Translation Document *(if applicable)*

_X_ Return Receipt Postcard (MPEP 503) (should be specifically itemized).

___ Other

**8. CORRESPONDENCE ADDRESS**

***CHRISTIE, PARKER & HALE, LLP, P.O. BOX 7068, PASADENA, CA 91109-7068***
**Customer Number: 23363**

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By Richard J. Paciulan
Richard J. Paciulan
Reg. No. 28,248
626/795-9900

RJP/cah

# FEE TRANSMITTAL
# UTILITY PATENT APPLICATION

**DATE: October 5, 2001**

Docket No. : 47426/RJP/B600
Inventor(s) : Myles H. Wakayama
Title : LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS

Duplicate __

## FEE DETERMINATION

| CLAIMS AS FILED | | | | | |
|---|---|---|---|---|---|
| | NUMBER FILED | NUMBER EXTRA | SMALL ENTITY RATE | LARGE ENTITY RATE | FEE |
| TOTAL CLAIMS | 1 – 20 | 0 | x $9.00 | x $18.00 | |
| INDEPENDENT CLAIMS | 1 – 3 | 0 | x $42.00 | x $84.00 | |
| MULTIPLE-DEPENDENT CLAIMS FEE | | | $140.00 | $280.00 | |
| BASIC FEE | | | $370.00 | $740.00 | $740.00 |
| | | | | TOTAL FILING FEE | $740.00 |
| List Independent Claims: 1 | | | | | |

## METHOD OF PAYMENT

_X_ No filing fee enclosed

_X_ No Deposit Account Authorization.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By Richard J. Paciulan
Richard J. Paciulan
Reg. No. 28,248
626/795-9900

RJP/cah
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PATENT

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**EXPRESS MAIL NO. EL 717376625 US**

| | | |
|---|---|---|
| Applicant | : | Myles H. Wakayama |
| Application No. | : | Not assigned |
| Filed | : | Herewith |
| Title | : | LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS |
| Docket No. | : | 47426/RJP/B600 |

## PRELIMINARY AMENDMENT

Post Office Box 7068
Pasadena, CA 91109-7068
October 5, 2001

Assistant Commissioner for Patents
Washington, D.C. 20231

Commissioner:

**In the Drawings**

Please replace Figs. 3 and 4 of parent application with amended Figs. 3 and 4 as indicated in the accompanying drawings.

**In the Claims**

Please cancel claims 2-23.

## REMARKS

The amendments submitted herewith are requested to be entered and included when the application is taken up for examination. Certain claims have been canceled since they were addressed in the parent application. Figs. 3 and 4 have been amended (marked in red) to indicate "Prior Art" to be consistent with a drawing amendment requested by the Examiner during the prosecution of the parent application.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By Richard J. Paciulan

Richard J. Paciulan
Reg. No. 28,248
626/795-9900

RJP/cah
CAH PAS385278 1-*-10/5/01 8 46 AM

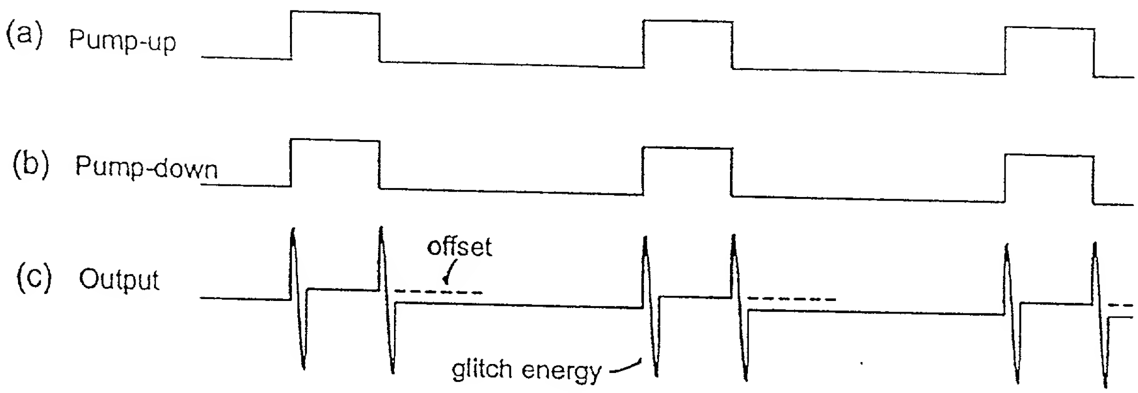


*FIG. 2*

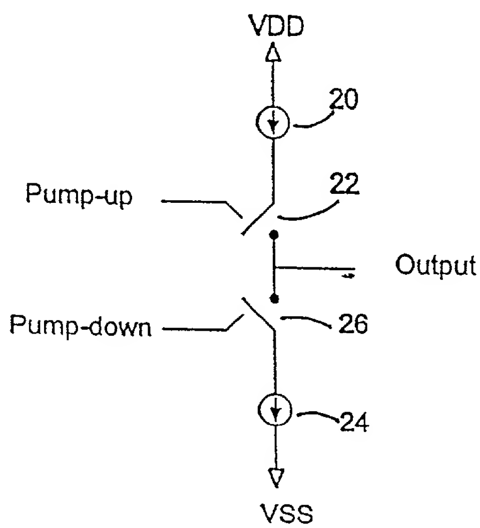


*FIG. 3*

PRIOR ART

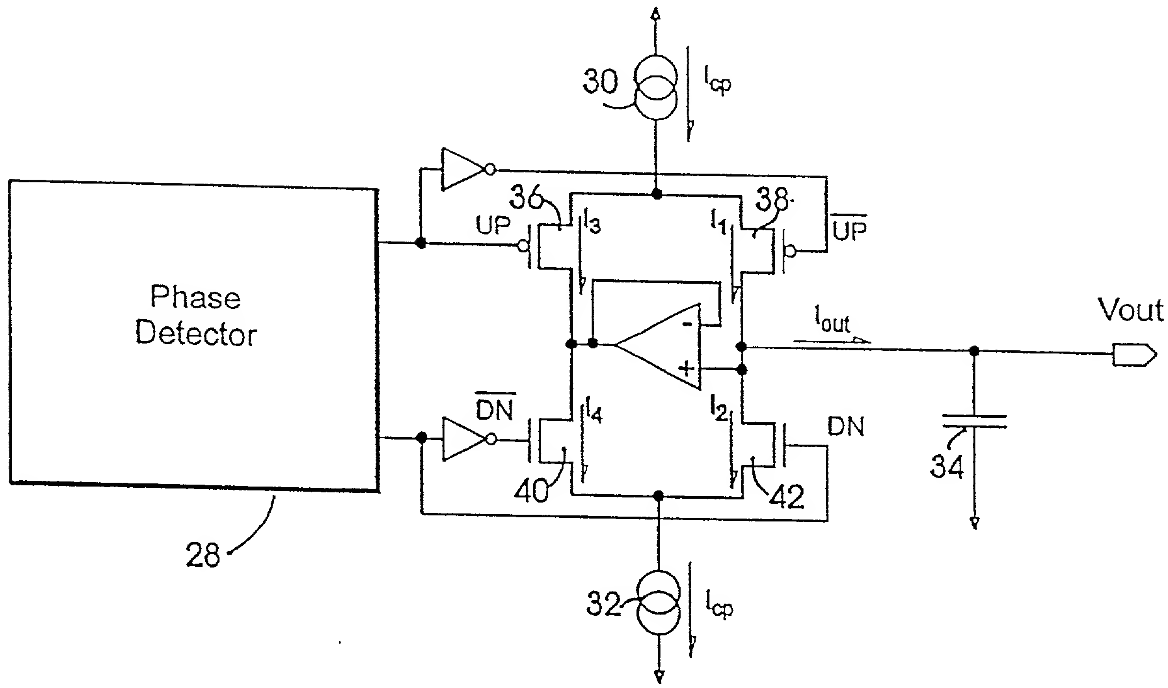


FIG. 4
PRIOR ART

# LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to co-pending provisional application Serial No. 60/101,555, filed September 21, 1998, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP DESIGN, commonly owned by the Assignee of the present invention.

## FIELD OF THE INVENTION

The present invention is directed to high speed data transmission and conversion systems and, more particularly, to a system for and a method of controlling the average current output of a charge pump such that glitch energy and offset voltage errors are minimized.

## BACKGROUND OF THE INVENTION

The past several years have witnessed a dramatic increase in the capabilities of high-speed, high-density, broadband data communication systems. Pertinent such systems range anywhere from broadcast or cablecast HDTV systems, local area and wide area (LAN, WAN) systems for multimedia, fibre to the home (FTTH) applications and board-to-board interconnections in exchange systems and computers.

In any one of the foregoing applications, it should be noted that bidirectional data communication is in digital form and, accordingly, clock and data recovery circuitry is a key component of the efficient functioning of modern data communications systems. The ability to regenerate binary data is an inherent advantage of transmitting information digitally as opposed to transmitting such information in analog form. However, in order for the intelligence signal to be correctly reconstructed at the receiving end, the transmitted binary data must be regenerated


Express Mail No. EL717376625US

with the fewest possible number of bit errors, requiring received data to be sampled at an optimum sample rate and at an optimum instance of time. Given the bandwidth constraints imposed on most modern data communication systems, it is generally impractical to transmit the requisite sampling clock signal separate from the transmitted datastream. Timing information is consequently derived from the incoming transmitted data signal itself. Extraction of the implicit timing signal is generally termed timing recovery (or clock recovery) in it's functional role in general digital receiver technology, is traditionally performed by a phase-lock-loop system such as that illustrated in FIG. 1.

Phase-lock-loops operate to compare the frequency and/or phase of an incoming serial datastream to a periodic reference clock signal generated by an oscillator circuit, and to adjust the operational frequency and phase characteristics of the oscillator until its output stream is "locked" in both frequency and phase to the data signal. A reference clock is thereby established which, in turn, controls operation of a decision circuit which regenerates (or retimes) the data signal. The phase-lock-loop suitably comprises a phase detector 10 whose output is coupled to a charge pump circuit 12, operatively connected, in turn, to a loop filter 13 and a voltage controlled oscillator (or VCO) 14.

The data signal is received at a data input of the phase detector 10, in which the occurrence of the data's rising edge (its phase) is compared in time to the occurrence of a rising edge (the phase) of an output signal of the VCO 14. Conventionally, the phase detector incorporates logic circuity (in effect a logical XNOR function) which precludes an output signal from being issued during phase comparisons unless two rising edges are present during a comparison cycle. This features prevents the phase-lock-loop from becoming unstable by

trying to perform a phase comparison between a VCO rising edge and a DATA ZERO bit (necessarily without a rising edge). It will be understood that the phase comparison result in such a situation would indicate either an infinite phase lead or an infinite phase lag, thus causing the VCO frequency to run out of control.

According to convention, the phase detector 10 issues a PUMP UP signal 16 to the charge pump 12 if the datastream phase leads the VCO signal, and issues a PUMP DN 18 if the datastream phase lags the VCO signal. PUMP UP and PUMP DN are directed to the charge pump 12 which sources or sinks a particular amount of current (the pump current) to or from, respectively, the loop filter 13. Voltage is developed as the pump current is sourced or sunk, with the voltage being used to control the operational frequency of the VCO 14. The sign of the VCO control voltage variation depends on whether the phase of the datastream leads or lags the phase of the VCO output and its magnitude is a function of the extent of the phase lead or phase lag. Thus, the operational frequency of the VCO 14 is increased or decreased, as appropriate, to reduce the phase lead or phase lag of the inputs to the phase detector 10. The phase-lock-loop thus ensures that the VCO output, which is used as a timing reference, is locked in phase with the incoming serial datastream. Once the PLL is "locked", the timing reference signal (i.e., the VCO output) is used to control operation of a decision circuit 16 which defines regenerated or retimed data.

A particular shortcoming of prior art phase-lock-loop systems is that the charge pump is required to source and sink current which precisely represents the magnitude and polarity of a phase difference between incoming data and the VCO. In addition, for a type II or a type IV phase detector operating in quasi flywheel mode, the charge pump is required to source and sink current in such a manner that the output current, averaged

over a correction cycle, equals 0. In other words, the charge pump should ideally only cause corrections to be made to the operating characteristics of the VCO which result from consistent frequency shifts of the datastream, such that the VCO is locked to the mean phase of the incoming datastream rather than to the phase of any specific data bit.

Maintaining perfect phase-lock VCO to data, however, is particularly difficult for conventional prior art-type phase-lock-loop circuits operating in the GHz range, because of the internal construction of conventional prior art-type charge pump circuits. In addition, the source and sink current waveforms, of such conventional charge pump circuits, exhibit significant amounts of offset and "glitch errors" which cause the source and sink current waveforms to be non-symmetrical. This non-symmetry necessarily results in a residual charge being left on the filter capacitor at the end of a correction cycle and further causes a non-zero increment to the control voltage $V_C$ to the VCO. The terms "offset" and "glitch errors" refer to fluctuations in the source and/or sink current waveforms and represent quantifiable departures from a smooth waveform characteristic. These fluctuations are caused by a variety of factors, the majority of which are functions of the physical and electrical properties of semiconductor integrated circuit transistors and integrated circuit charge pumps manufactured therefrom and exhibit the response characteristics illustrated in FIG. 2.

Offset is an undesirable quantum of charge output from a charge pump when the PUMP UP and PUMP DN signals applied to the input of the charge pump are identical (i.e., the output of the charge pump should be flat or zero). This DC offset current tends to perturb the system in one direction or the other and results in timing jitter at the output of the VCO. Glitch energy is a sharp transition peak signal defined at the output of the

charge pump, caused in major part by transition edge (clock) feed through effects of the input signals.

To better understand the causes of offset and glitch errors, it will be helpful to review the common and well-known charge pump architecture depicted in simplified form in FIG. 3.

Conceptually, a charge pump may be viewed as a "pump up" current source 20 connected in series with a switch 22 to provide an output source current in response to a PUMP UP signal issued by a, for example, phase detector. Similarly, a "pump down" current sink 24 is coupled between a $V_{SS}$ supply and a second switch 26 which, together function to define a sink current in response to a PUMP DN signal from the phase detector. While relatively simple, the simplified charge pump design of FIG. 3 can be used to illustrate several practical problems with contemporary charge pump design. For example, DC mismatches in the up and down current sources 20 and 24 necessarily cause a DC offset in the charge pump output when both PUMP UP and PUMP DN activate the respective switches 22 and 26, at the same time.

Likewise, the voltage node between the current source 20 and switch 22 on the "UP" side of the charge pump will rise to $V_{DD}$ when the pump-up switch 22 is in an open condition. The voltage node between the current sink 24 and switch 26 on the pump-down side of the charge pump will go to $V_{SS}$ when the pump-down switch is in an open condition. These conditions cause a DC offset in the charge pump output that is necessarily dependent on the output voltage because of well-known parasitic capacitance effects that are present on the above-described nodes. In addition to the offset effects inherent in contemporary charge pump designs, it will be understood that as the switches 22 and 26 open and close in response to PUMP UP and PUMP DN signals issued by the phase detector, voltage spikes, ground bounce, and the like, will cause a sharp "ring" spike at transition edge instants. Spikes, ringing and other non-linearities introduced

by switch transients, clock feed through effects, and the like, are subsumed into the term "glitch energy".

Accordingly, prior art-type charge pump circuits do not provide a smooth, constant and symmetrical response characteristic between their source and sink currents during phase lock, thus introducing variation to the loop filter and, consequently the VCO output. This variability becomes proportionately more significant as the VCO frequency increases. Accordingly, for high-speed phase-lock-loops, there is a demonstrated need for a high precision charge pump which is designed and constructed such that glitch errors and DC offsets are minimized for both source and sink phases of a detection cycle, such that the average current, integrated across the cycle, more closely approximates zero.

## SUMMARY OF THE INVENTION

A high-speed phase lock loop circuit includes a high precision charge pump which functions to maintain the stability of VCO lock by providing source and sink pump currents which are substantially zero over phase correction cycle. The uniformity of source and sink currents is imposed by valuating the voltages at the common drain nodes of the charge pump's first and second parallel conduction paths by a feedback element. The feedback element controls the value of an "adjust" current source so as to drive the two common drain nodes to an equi-potential level.

In one aspect of the invention, a phase lock loop includes a phase/frequency detector for comparing a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal developed by a voltage controlled oscillator (VCO), numerically controlled oscillator (NCO) or the like. A charge pump sources and sinks characteristic current in response to control signals developed by the phase/frequency detector, in response to a phase or

frequency comparison event. The charge pump is constructed of two parallel current paths, each a mirror image of the other, and both coupled between a pump-up current source and a pump-down current source.

Each of the two parallel current paths is constructed of an upper switch connected in series with a lower switch with the common nodes of each parallel current path defining a respective output node. The upper switch may be constructed of an N-channel transistor, while the lower switch may be constructed of a P-channel transistor. The charge pump includes a feedback element coupled between the output nodes and an "adjust" current source which functions to balance currents in the two parallel current paths so as to minimize DC offsets at the circuit output.

In a further aspect of the invention, a first output node defined by the common nodes of the upper and lower switches defining one of the parallel current paths is coupled to a loop filter, connected between the charge pump and a VCO. The loop filter develops a control voltage for the VCO in response to a characteristic current sourced or sunk by the charge pump and received from the first output node. The loop filter includes an RC network coupled between the charge pump's first output node and a reference potential, and including a resistor element in series with a first capacitor defining a zero of the filter.

In an additional aspect of the invention, the charge pump includes a second output node defined by the common nodes of the upper and lower switches defining a second one of the parallel current paths. The second output node is coupled to a reference potential through a third "dump" capacitor having a value substantially the same as the "zero" capacitor coupled to the first output node.

An amplifier, such as a transconductance amplifier, has first and second inputs coupled, respectively, to the first and second output nodes and an output connected to control operation

of an "adjust" current source. The "adjust" current source might be provided separately or, might be incorporated into the charge pump's "pump-up" or "pump-down" current sources directly. The amplifier thus forces the common drain nodes of each of the current paths to be maintained at an equi-potential value with respect to one another. By maintaining the dump capacitor node and the zero capacitor node at the same voltage during operation of the charge pump, independent of the output voltage of the charge pump, non-linearities and DC offsets developed by the charge pump are minimized.

## DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present invention will be more fully understood when considered with respect to the following detailed description, appended claims, and accompanying drawings, wherein:

FIG. 1 is a semi-schematic simplified block diagram of a phase-lock-loop, configured to provide timing information to a decision circuit;

FIG. 2 is a series of waveform diagrams illustrating the effects of glitch energy and DC offset on the output of a charge pump;

FIG. 3 is a semi-schematic simplified circuit diagram of a conventional charge pump design;

FIG. 4 is a semi-schematic simplified circuit diagram of a charge pump and loop filter coupled to a phase detector in accordance with the prior art;

FIG. 5 is a simplified semi-schematic circuit diagram of a low offset and low glitch energy high precision charge pump in accordance with the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

In practical terms, lack of perfect symmetry between sourced and sunk charge pump current selectively adds a small component (a DC offset component, a glitch error component, or both) to the control voltage $V_C$ provided to a VCO. These error components selectively shift frequency of a VCO relative to its nominal center frequency. Any offset from the center frequency will cause a phase detector's data capture window to shift, thus allowing a portion of data pulse position distribution to fall out side the detection window, and consequently increasing the system's bit error rate.

FIG. 4 illustrates, in simplified semi-schematic circuit diagram form, a typical prior art-type three-state charge pump, coupled to receive PUMP UP and PUMP DN signals from a phase detector 28. The charge pump is implemented as two switched current sources 30 and 32 driving a capacitor 34 which, in turn, defines an output voltage ($V_{OUT}$ or $V_C$). The charge pump switches are disposed as an upper and lower switch bank, the upper switch bank constructed of a pair of P-channel transistors 36 and 38 coupled at their source terminals to an upper current source 30 and whose drains are connected to the drains of a corresponding pair of N-channel transistors 40 and 42 which define the lower switch bank. The lower switch bank transistors have their source terminals connected in common and to the second current source 32. For purposes of explanation, it will be assumed that the upper current source 30 is implemented with PFETs and the lower current source 32 is implemented with NFETs, according to well understood design principles.

In operation, a PUMP UP pulse of characteristic width T would cause a positive output current $+I_{CP}$ to deposit a charge equal to ($I_{CP}T$) on the capacitor 34 of a, for example, loop filter. Likewise, a PUMP DN pulse of width T would cause a negative current $-I_{CP}$ to remove a charge equal to ($I_{CP}T$) from the filter capacitor 34. Thus, in the case of a phase difference,

either a positive charge would steadily accumulate on the capacitor, yielding an infinite DC gain for the phase detector, or charge will be steadily removed from the capacitor on every phase comparison, driving DC gain toward negative infinity. In the third state, i.e. "lock" the steady state gain is desirably zero.

An important implication to this type of charge pump design is that offsets and mismatches between the PUMP UP and PUMP DN switch transistors would result in currents being either sourced to or sunk from the capacitor even though the phase detector experiences zero static phase difference at the inputs. Mismatch error is introduced in the behavior of prior art-type charge pumps by implementing the current source switches from different transistor types, i.e., N-channel and P-channel transistors. When these switches turn-off, charge injection and feed-through mismatch, inherent in the different physical properties of P-channel and N-channel transistors, results in an error step at the output which, when fed through the loop filter, perturbs the VCO frequency until the next phase comparison cycle. Moreover, when the switches are turned-off, the upper and lower pump currents generated by the respective current sources 30 and 32, pull their respective source nodes to VDD and ground causing charge-sharing between the capacitor 34 and the internal parasitic capacitances of the various transistors, when the switches are once again turned-on. Since the internal parasitic capacitances of N-channel and P-channel transistors are significantly different, the output is significantly disturbed at turn-on. In addition to disturbing the output at turn-on, the well understood parametric differences between N-channel and P-channel transistors necessarily results in the quantifiable glitches introduced at the output, for PUMP UP and PUMP DN, to be different. Consequently, the average output current is non-zero, i.e., contains a DC offset.

A high precision charge pump configured for use in very high speed applications, such as data and timing recovery circuitry in broadband data communication systems, is depicted in the simplified semi-schematic circuit diagram of FIG. 5. The charge pump, in accordance with the present invention, is seen to be somewhat similar to the conventional charge pump described with reference to FIG. 4, but differs from the prior art design in several significant aspects.

The high precision charge pump, indicated generally at 40 will be understood to be constructed of two parallel current paths, each a mirror image of the other, and both coupled between a pump-up current source 42, connected in turn to VDD, and a pump-down current source (current sink) 44 coupled to VSS.

First current path, i.e., the left current path, is constructed of an upper switch, illustrated in the exemplary embodiment as a P-channel transistor 46, connected in series with a lower switch, illustrated in the exemplary embodiment as an N-channel transistor 48. It should be understood that the active elements according to the invention are current switches , and are only represented as MOSFET transistors for ease of explanation. Likewise, whether the transistors are N-channel or P-channel, is a matter of design choice. One having skill in the art of circuit design will be able to make the appropriate substitutions while still gaining the benefits of the present invention.

Similarly, the second current path, the right current path, is constructed of an upper P-channel transistor 50 and a lower N-channel transistor 52. The P-channel transistors 46 and 50 are Source mirror images of one another and have their drain terminals connected together in common and to the pump-up current source 42. The lower N-channel transistors 48 and 52 are likewise mirror images of one another and also have their source terminals

connected together in common and to the pump-down current source 44.

The gate terminals of the matched N-channel transistors 48 and 52 are configured to be operatively responsive to a PUMP DN signal received from a phase detector, for example. One of the matched N-channel transistors has its gate terminal coupled directly to the PUMP DN signal while the other matched N-channel transistor has its gate terminal coupled to receive the inverse of the PUMP DN signal, which might be implemented by directing PUMP DN through an inverting buffer. Thus, the gate terminal of one of the matched N-channel transistors is coupled to DN, while the gate terminal of the second matched N-channel transistor is coupled to $\overline{DN}$.

In like fashion, the matched pair of P-channel transistors 46 and 50 are connected to be operatively responsive to the PUMP UP signal with the gate terminal of one of the matched P-channel transistors connected to UP and the gate terminal of the second matched P-channel transistor receiving $\overline{UP}$. $\overline{UP}$ is generated by directing UP through an inverting buffer and thence to the gate terminal of the P-channel transistor.

An output node is defined by the common drain nodes of the P-channel and N-channel transistors defining one of the parallel current paths. Source and sink currents are output to an analog loop filter 54 constructed to include an RC network characterized by a resistor element 56 and a capacitor 58 which define the filters zero. The RC network is coupled between the charge pump output and ground in parallel with a second capacitor 60 which defines the analog loop filter's pole.

An amplifier, such as a transconductance (gm) amplifier 62 has a first input connected to a node defined between the resistor element 56 and zero capacitor 58 of the loop filter's RC network. A second input of the transconductance amplifier 62 is connected to a second output node defined by the common drain

terminals of the second parallel conduction path of the charge pump. A dump capacitor 64 is coupled between the second input of the transconductance amplifier 62 and a reference potential in a manner similar to and consistent with the loop filter's zero capacitor 58 and the first input of the transconductance amplifier 62. Thus, the two inputs of the transconductance amplifier will be understood to be in static balance with respect to one another, given the appropriate design values for the dump capacitor 64 and zero capacitor 58.

The output of the transconductance amplifier 62 is coupled to control a third current source 63 which is connected in parallel fashion to the "down" current source 44 between the transistor elements of the charge pump and VSS. Third current source 63 is constructed to conduct an "adjust" current which is nominally zero, and is further constructed to have a limited current conduction range relative to the "down" current source 44.

In operation, the transconductance amplifier 62 functions as a feedback element to drive the dump capacitor node (i.e., the second output node of the charge pump) to the same voltage value as the zero capacitor node, by controlling the value of the "adjust" current source 63. Since the "adjust" current is nominally zero (i.e., the circuit is balanced) the transconductance amplifier 62 requires very little additional power to operate. By maintaining the dump capacitor node and the zero capacitor node at the same voltage during operation of the charge pump, independent of the output voltage of the charge pump, non-linearities and DC offsets developed by the transistor's parasitic capacitances are minimized.

Further, the transconductance amplifier 62 forces the common drain nodes of each of the current paths of the charge pump 40 to be maintained at an equi-potential value with respect to one another. Thus, transconductance amplifier in combination with

the "adjust" current source 63 functions to force the "down" current sunk by the "down" current source 44 to exactly equal the "up" current sourced by the "up" current source 42, in a manner independent of the output voltage of the charge pump. Thus, any DC mismatches between the "up" and "down" current sources which could cause offsets in the charge pump output, are removed. Since the charge pump output nodes are maintained at an equi-potential level, there is no further voltage dependence of the "up" and "down" current sources on the output voltage and further minimized DC offsets in the charge pump output. are minimized

It should be realized by one having skill in the art that the thrid "adjust" current source 63 need not be provided neither as a separate element, nor in parallel with the "down" current source. The "adjust" current source might also be partially or wholly provided in parallel with the "pump-up" current source 42. Further, the "adjust" current source might be eliminated as a separate element and the amplifier 62 configured to control either the "pump-up" 42 or "pump-down" current sources directly.

A high-speed phase lock loop circuit has been described and includes a high precision charge pump circuit with low offset and low glitch energy which functions to maintain the stability of VCO lock by providing source and sink pump currents which are substantially zero over a phase correction cycle. The uniformity of source and sink currents is imposed by evaluating the voltages at the common drain nodes of the charge pump's first and second parallel conduction paths by a feedback element. The feedback element controls the value of an "adjust" current source so as to drive the two common drain nodes to an equi-potential level.

It will be understood that the "adjust" current source can be implemented as an independent current source which has a limited range relative to the "down" current source or it can be implemented in conjunction with the "down" current source as a secondary element controlled by the charge pump's feedback

element. Likewise, the feedback current may be applied to the "up" current source instead of, or in conjunction with the "down" current source.

While the invention has been described in terms of CMOS integrated circuit technology, it will be evident to one having skill in the art that the invention may likewise be suitably implemented in other semiconductor technologies, such as bipolar, bi-CMOS, and the like. Moreover, the circuit according to the invention may be constructed from discrete components as opposed to a monolithic integrated circuit, so long as the individual components are matched as closely as possible to one another.

It will thus be recognized by those skilled in the art that various modifications may be made to the illustrated and other embodiments of the invention described above, with out departing from the broad inventive scope thereof. It will be understood, therefore, that the invention is not limited to the particular embodiments or arrangements disclosed, but is rather intended to cover any changes, adaptations or modifications which are within the scope and spirit of the invention as defined by the appended claims.

CLAIMS

1. A phase lock loop comprising:

a detector for comparing a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal;

a timing reference signal generator, connected in feedback fashion to provide a timing reference signal to the detector; and

a charge pump connected to receive control signals developed by the detector, the charge pump sourcing and sinking a characteristic current in response to the control signals, the charge pump constructed of two parallel current paths, each a mirror image of the other, and both coupled between a pump-up current source and a pump-down current source, wherein the charge pump includes feedback means coupled between an output and an adjustment current source, the feedback means operative to balance currents in the two parallel current paths so as to minimize DC offsets at the output.

2. The phase lock loop according to claim 1, each of the two parallel current paths constructed of an upper switch connected in series with a lower switch, the common nodes of each parallel current path defining an output node.

3. The phase lock loop according to claim 2, further comprising a loop filter coupled between the charge pump and the timing reference generator, the loop filter developing a control voltage for the timing reference generator in response to a characteristic current sourced or sunk by the charge pump.

4. The phase lock loop according to claim 3, wherein a first output node defined by the common nodes of the upper and

lower switches defining one of the parallel current paths is coupled to the loop filter.

5. The phase lock loop according to claim 4, the loop filter including an RC network having a resistor element in series with a first capacitor, together defining a zero of the filter, the RC network coupled between the charge pump's first output and a reference potential in parallel with a second capacitor defining a pole of the filter.

6. The phase lock loop according to claim 5, the charge pump including a second output node defined by the common nodes of the upper and lower switches defining a second one of the parallel current paths, the second output node coupled to a reference potential potential through a third capacitor.

7. The phase lock loop according to claim 6, feedback means including an amplifier, the amplifier having a first input coupled to a node defined between the resistor element the zero capacitor of the loop filter's RC network, the amplifier having a second input connected to the second output node defined by the common nodes of the second parallel conduction path of the charge pump.

8. The phase lock loop according to claim 7, the amplifier including an output, the output controlling operation of an adjust current source, the amplifier and adjust current source in combination maintaining the charge pump's second output node at the same voltage as the first output node independent of the operational state of the charge pump.

9. The phase lock loop according to claim 8, each upper switch comprising a P-channel transistor.

10. The phase lock loop according to claim 9, each lower switch comprising an N-channel transistor.

11. The phase lock loop according to claim 10, wherein the amplifier comprises a transconductance amplifier.

12. A feedback controlled timing circuit, comprising:

a comparison circuit configured to compare a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal, the comparison circuit asserting control signals in response to said comparison;

a timing reference signal generator, connected to provide a timing reference signal to the comparison circuit, the timing reference signal generator responsive, in feedback fashion, to said control signals asserted by the comparison circuit; and

a charge pump coupled between the comparison circuit and the timing reference signal generator, the charge pump sourcing and sinking a characteristic current in response to the control signals, the charge pump constructed of two parallel current paths, each including an upper switch connected in series with a lower switch, the common nodes of each parallel current path maintained at an equi-potential value with respect to one another so as to minimize DC offsets of the output.

13. The timing circuit according to claim 12, each of the parallel current path's common nodes defining an output, one such output coupled to a loop filter.

14. The timing circuit according to claim 13, the loop filter including an RC network having a resistor element in series with a first capacitor, together defining a zero of the

filter, the RC network coupled between the charge pump's first output and a reference potential.

15. The timing circuit according to claim 14, the charge pump including a second output node coupled to the reference potential through a dump capacitor.

16. The timing circuit according to claim 15, the two parallel current paths coupled between a first pump-up current source and a second pump-down current source.

17. The timing circuit according to claim 16, further comprising a two-input feedback element, each input connected to a respective one of the charge pump's two outputs, the feedback element further including an output coupled to control an adjust current source.

18. The timing circuit according to claim 17, the feedback element controlling a value of the adjust current source so as to drive the dump capacitor node to the same voltage value as the zero capacitor node, thereby maintaining the common nodes of each of the current paths of the charge pump at an equi-potential value with respect to one another.

19. The timing circuit according to claim 18, wherein the feedback element comprises a transconductance amplifier.

20. The timing circuit according to claim 18, each upper switch comprising a P-channel transistor.

21. The timing circuit according to claim 20, each lower switch comprising an N-channel transistor.

22. The timing circuit according to claim 21, wherein the adjust current source is incorporated into the pump-down current source.

23. The timing circuit according to claim 21, wherein the adjust current source is incorporated into the pump-up current source.

35870/JWE/B600

ABSTRACT OF THE DISCLOSURE

LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS

A high precision charge pump used in a phase-lock-loop incorporating a phase/frequency detector is designed and constructed to substantially eliminate the effects of DC offset and glitch errors on the charge pump output current. The high precision charge pump is constructed of parallel current paths each having a central node which is, in turn, connected to a feedback element. The feedback element defines a feedback current which is applied to the charge pump so as to maintain the two common drain nodes at an equi-potential level and to maintain the value of the pump-down current exactly equal to the value of the pump-up current output by the device.

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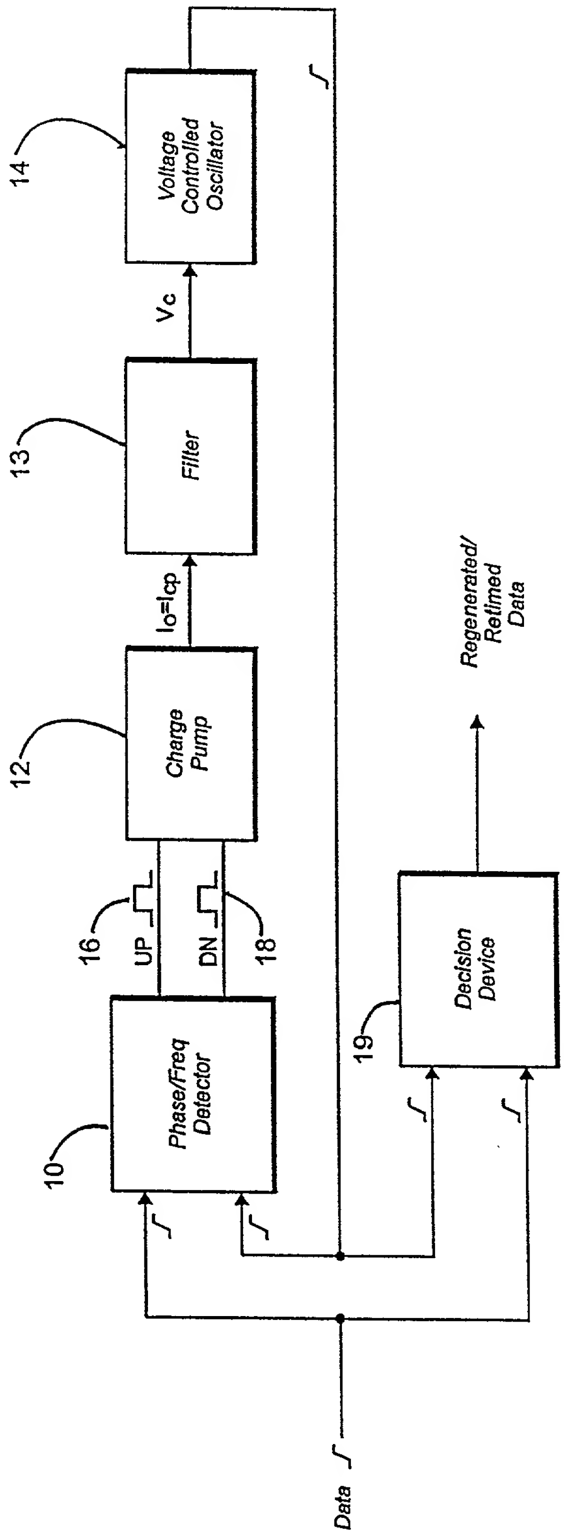


FIG. 1
(Prior Art)

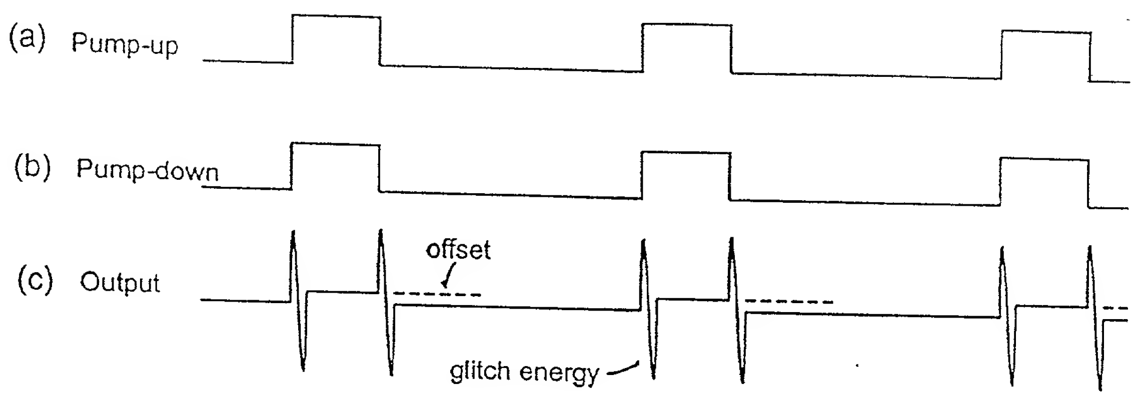


*FIG. 2*

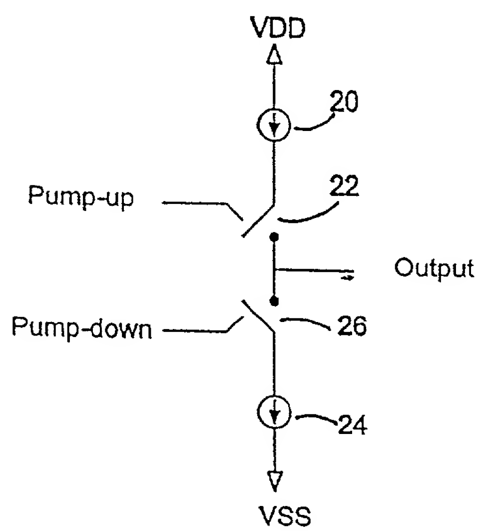


*FIG. 3*
*PRIOR ART*

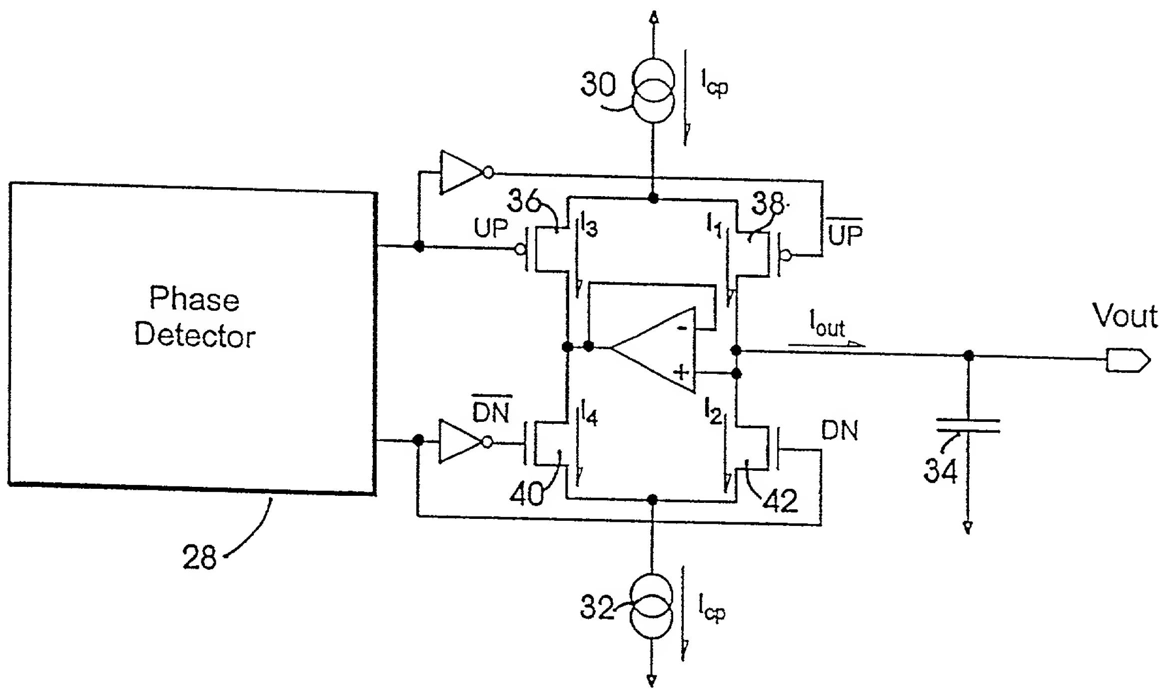


*FIG. 4*
*PRIOR ART*

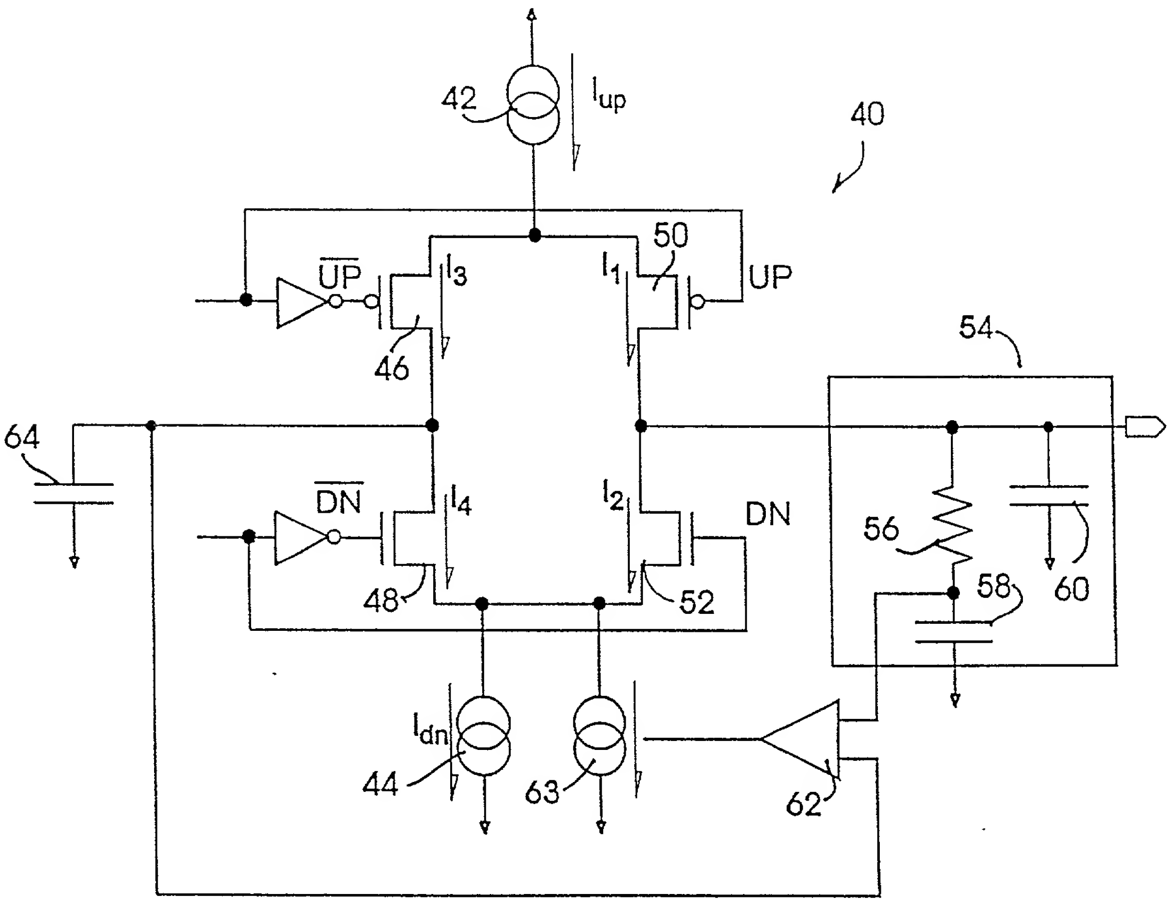
42
$I_{up}$
40
50
$\overline{UP}$
$I_3$
$I_1$
UP
46
54
64
$\overline{DN}$
$I_4$
$I_2$
DN
56
58
60
48
52
$I_{dn}$
44
63
62

*FIG. 5*

## DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATIONS

PATENT

Docket No. : 35870/JWE/B600

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS, the specification of which is attached hereto unless the following is checked:

__ was filed on __ as United States Application Number or PCT International Application Number __ and was amended on __ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of the foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

| Application Number | Country | Filing Date (day/month/year) | Priority Claimed |
|---|---|---|---|

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

| Application Number | Filing Date |
|---|---|
| 60/101,555 | September 21, 1998 |

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

| Application Number | Filing Date | Patented/Pending/Abandoned |
|---|---|---|

POWER OF ATTORNEY: I hereby appoint the following attorneys and agents of the law firm CHRISTIE, PARKER & HALE, LLP to prosecute this application and any international application under the Patent Cooperation Treaty based on it and to transact all business in the U.S. Patent and Trademark Office connected with either of them in accordance with instructions from the assignee of the entire interest in this application; or

## DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATIONS

**Docket No. 35870/JWE/B600**

from the first or sole inventor named below in the event the application is not assigned; or from __ in the event the power granted herein is for an application filed on behalf of a foreign attorney or agent.

| | | | | | |
|---|---|---|---|---|---|
| R. W. Johnston | (17,968) | John D. Carpenter | (34,133) | Lucinda G. Auciello | (42,270) |
| D. Bruce Prout | (20,958) | David A. Plumley | (37,208) | Norman E. Carte | (30,455) |
| Hayden A. Carney | (22,653) | Wesley W. Monroe | (39,778) | Joel A. Kauth | (41,886) |
| Richard J. Ward, Jr. | (24,187) | John W. Eldredge | (37,613) | Patrick Y. Ikehara | (42,681) |
| Russell R. Palmer, Jr. | (22,994) | Gregory S. Lampert | (35,581) | Mark Garscia | (31,953) |
| LeRoy T. Rahn | (20,356) | Grant T. Langton | (39,739) | Gary J. Nelson | (44,257) |
| Richard D. Seibel | (22,134) | Constantine Marantidis | (39,759) | Raymond R. Tabandeh | (43,945) |
| Walter G. Maxwell | (25,355) | Daniel R. Kimbell | (34,849) | Phuong-Quan Hoang | (41,839) |
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| David A. Dillard | (30,831) | Syed A. Hasan | (41,057) | Kathy Mojibi | (41,409) |
| Thomas J. Daly | (32,213) | Kathleen M. Olster | (42,052) | Cynthia A. Bonner | (P-44,548) |
| Vincent G. Gioia | (19,959) | Daniel M. Cavanagh | (41,661) | | |
| Edward R. Schwartz | (31,135) | Molly A. Holman | (40,022) | | |

The authority under this Power of Attorney of each person named above shall automatically terminate and be revoked upon such person ceasing to be a member or associate of or of counsel to that law firm.

**DIRECT TELEPHONE CALLS TO : John W. Eldredge, 626/795-9900**

**SEND CORRESPONDENCE TO : CHRISTIE, PARKER & HALE, LLP**
**P.O. Box 7068, Pasadena, CA 91109-7068**

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

| Full name of sole or first joint inventor | Inventor's signature | Date |
|---|---|---|
| Myles H. Wakayama | Myles H. Wakayama | 9/13/99 |
| **Residence and Post Office Address** | | **Citizenship** |
| 16 Windham Lane, Laguna Niguel, California 92677 | | U.S. |

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